REMARKS

This responds to the Office Action mailed on October 30, 2007.

Claims 1, 5, 8, 12, 16, and 21 are amended and no claims are canceled or added; as a result, claims 1-25 remain pending in this application.

§102 Rejection of the Claims

Claims 1-25 were rejected under 35 USC § 102(e) as being anticipated by Moyes et al. (U.S. 7,065,688; hereinafter "Moyes"). Applicant respectfully traverses the rejection of claims 1-25 for the same reasons as in the previous response. However, in view of the Response to Arguments section of the Final Office Action, Applicant has amended independent claims 1, 5, 8, 12, 16, and 21 to clarify the patentable nature of the claims.

In view of the Response to Arguments section of the Final Office Action, Applicant believes the Examiner understood the arguments made in the last response. As a result, Applicant reiterates those arguments and incorporates them herein by reference for the sake of brevity. However, to summarize those arguments, Moyes performs parallel memory initialization at the processor level while the present claims parallelize memory initialization and testing at the memory module level.

Applicant refers the examiners attention to FIG. 1 which illustrates how the processor 102 is distinct from the memory controller 104. Further, the memory modules 112, 114, 116 are distinct from the memory controller 104. Applicant's specification provides description as to the details of a processor in the paragraph beginning on line 17 of page 4. Description of the memory controller is found in the paragraph beginning at line 28 of page 4 and the following paragraphs. Description of the memory modules is found in the paragraph beginning at line 22 of page 5 and the following paragraphs. These descriptive portions of the specification, among others, provide background and definitions for the elements of the claims and highlight how the memory initialization and testing is performed by memory modules in response to commands originating with a processor and may be communicated via a memory controller. Further, FIG. 2, and its description beginning at line 7 of page 8, illustrates how a memory module includes memory storage units.

Applicant respectfully submits that this highlights what a memory module, as included in the claims, is and is not. A memory module is not a memory controller or a processor as is described in Moyes. Further, a memory module may include memory storage units, but is more than a portion of system memory. Thus, Applicant submits that the concept of a memory module is not disclosed, taught, or suggested in any manner within Moyes. A memory module, as claimed, provides an additional level of memory management and allows for finer grained parallel memory initialization and testing.

Applicant therefore respectfully submits that claims 1-25 are patentable over Moyes because Moyes fails to contemplate initialization or testing of memory via a memory module and Moyes performs parallel memory initialization at the processor level while the present claims parallelize memory initialization and testing at the memory module level. Thus, Applicant respectfully requests withdrawal of the 35 U.S.C. § 102(e) rejections and allowance of claims 1-25.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of

priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

By /Ann M. McCrackin/
Ann M. McCrackin
Reg. No. 42,858